

FIGURE 1A

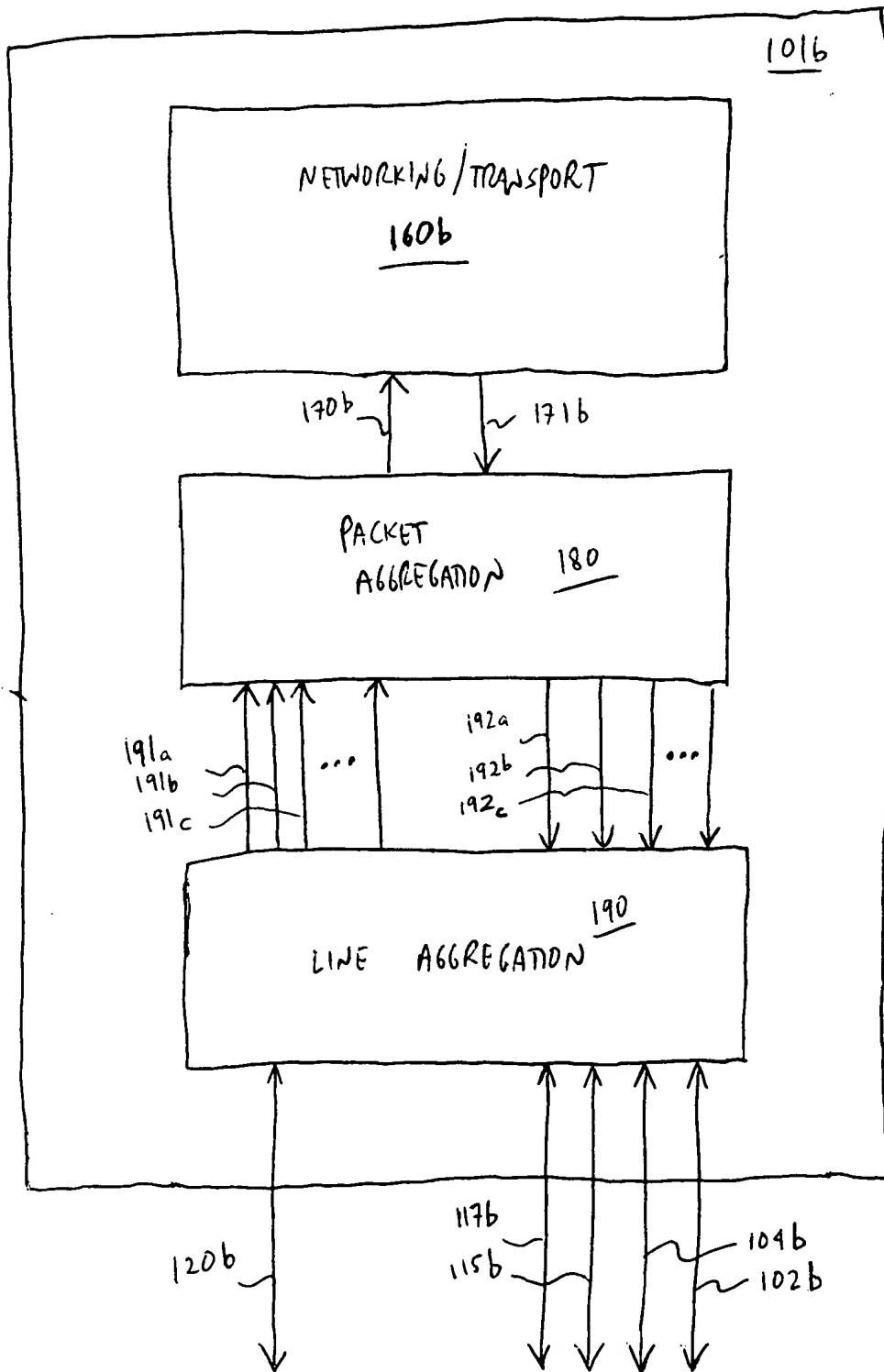


FIGURE 1B

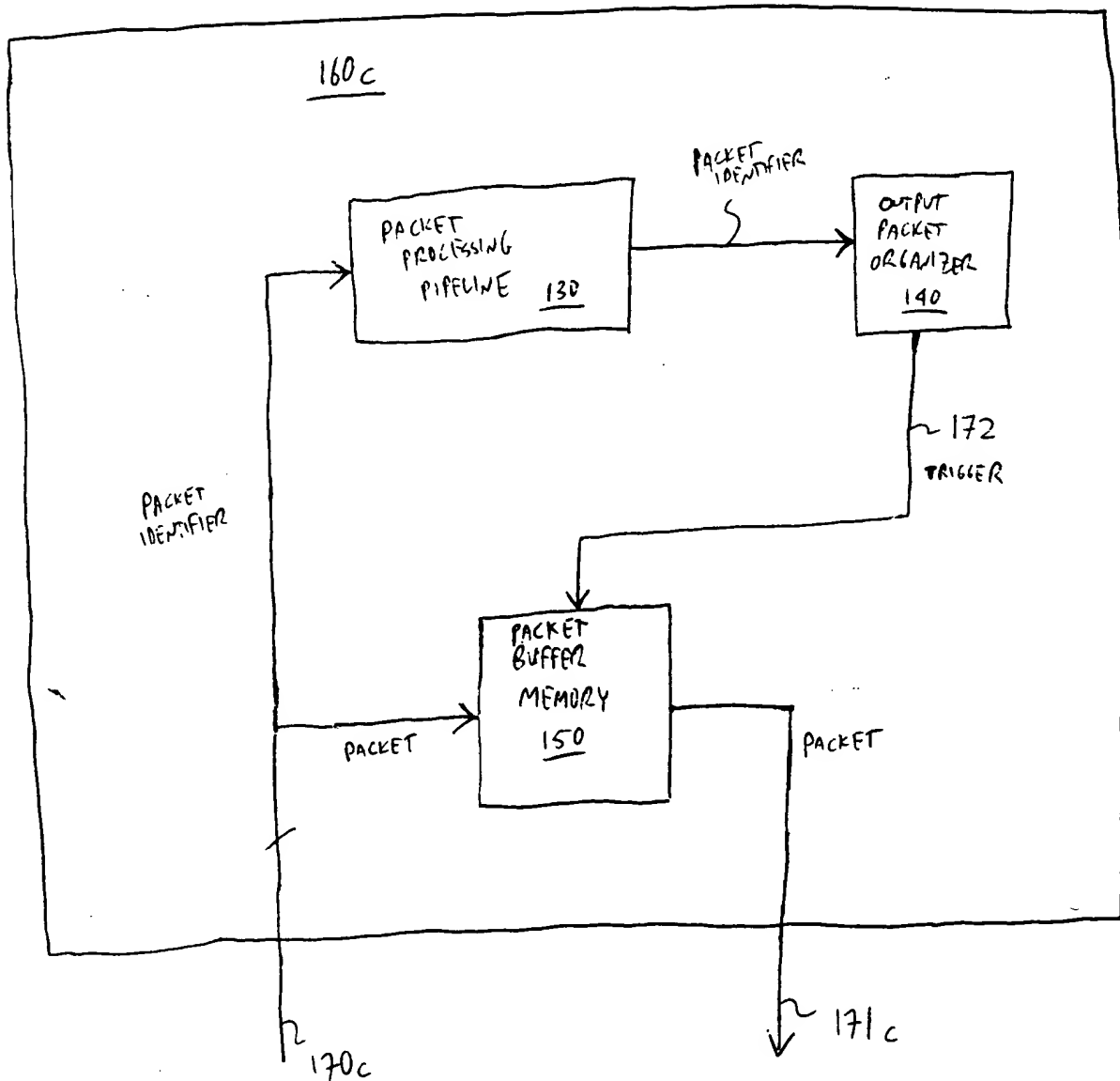
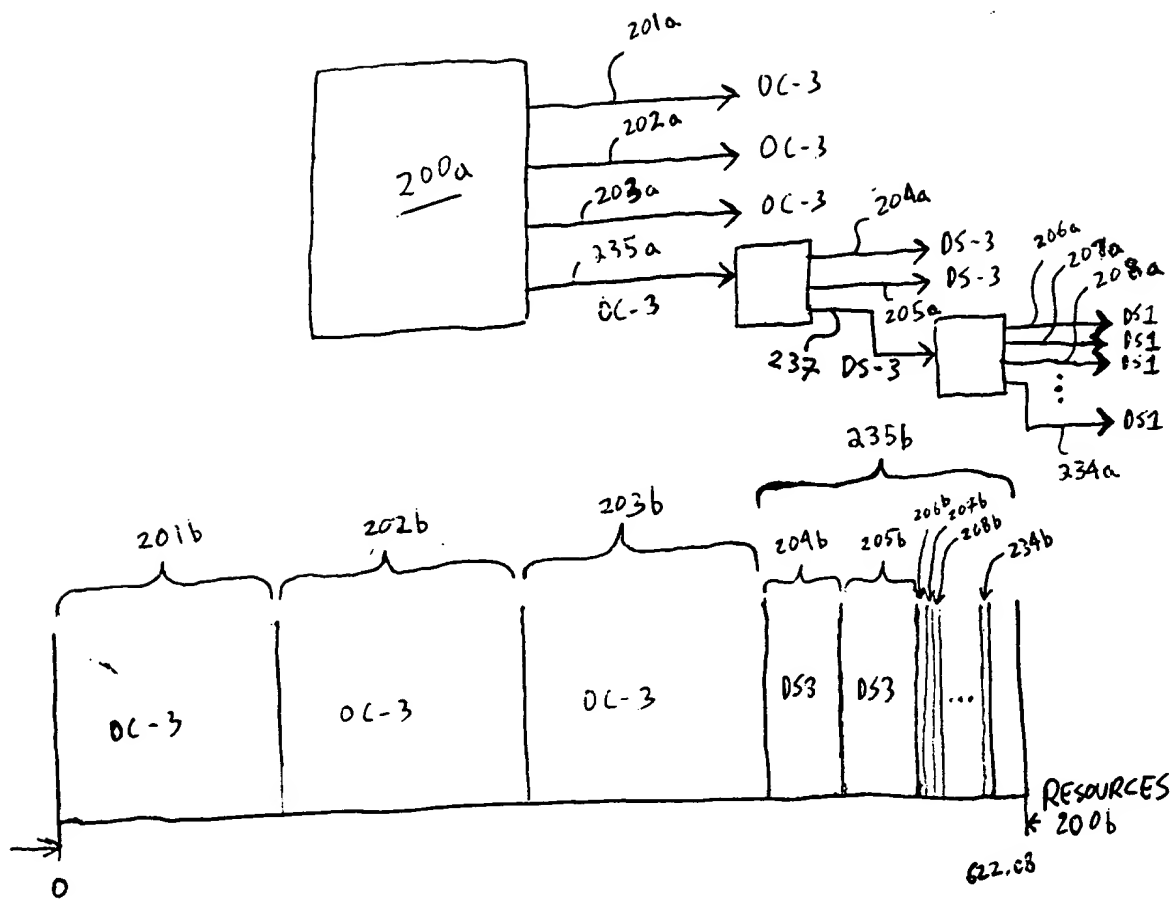
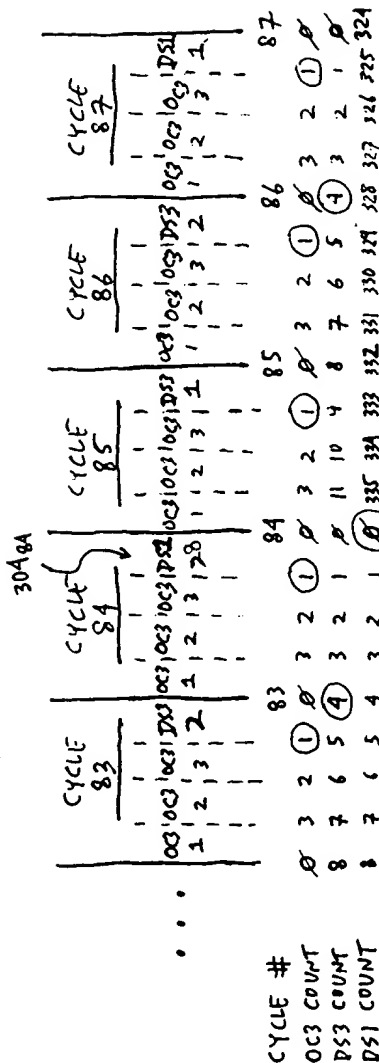
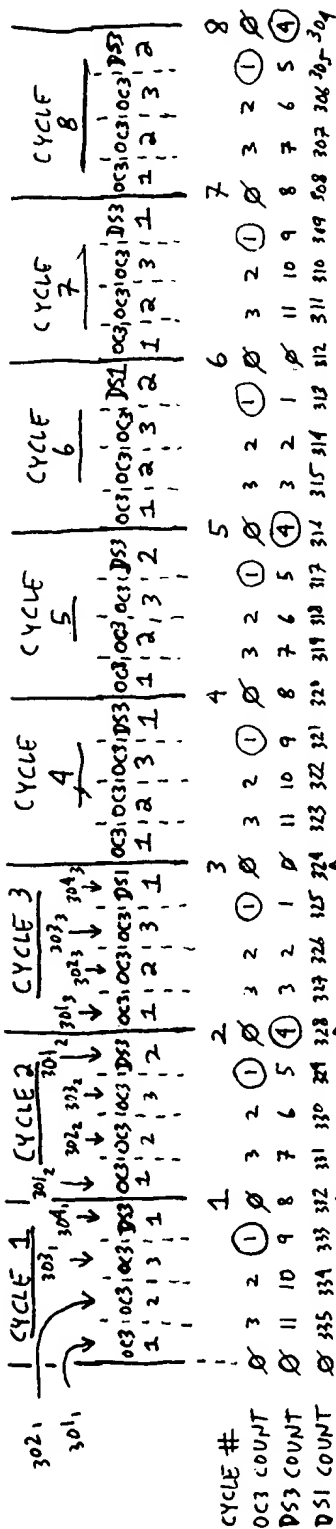


FIGURE 1c



When data, address, status, or control signals are active, the bus is in a high state. When the bus is in a low state, the bus is in a low state.



(X) = done bit received

FIGURE 3

500a

	DATA ENTRY				
	ADDR	LINK POINTER	PID	DONE BIT	
PORT 1	501	502	PID ₁	0	OC3_1
PORT 2	502	503	PID ₂	0	OC3_2
PORT 3	503	501	PID ₃	1	OC3_3
PORT 4	504	505	PID ₄	0	DS3_1
PORT 5	505	504	PID ₅	1	DS3_2
PORT 6	506	507	PID ₆	0	DS1_1
PORT 7	507	508	PID ₇	0	DS1_2
PORT 32	532	533	PID ₃₂	0	DS1_27
PORT 33	533	506	PID ₃₃	1	DS1_28

FIG. 5A

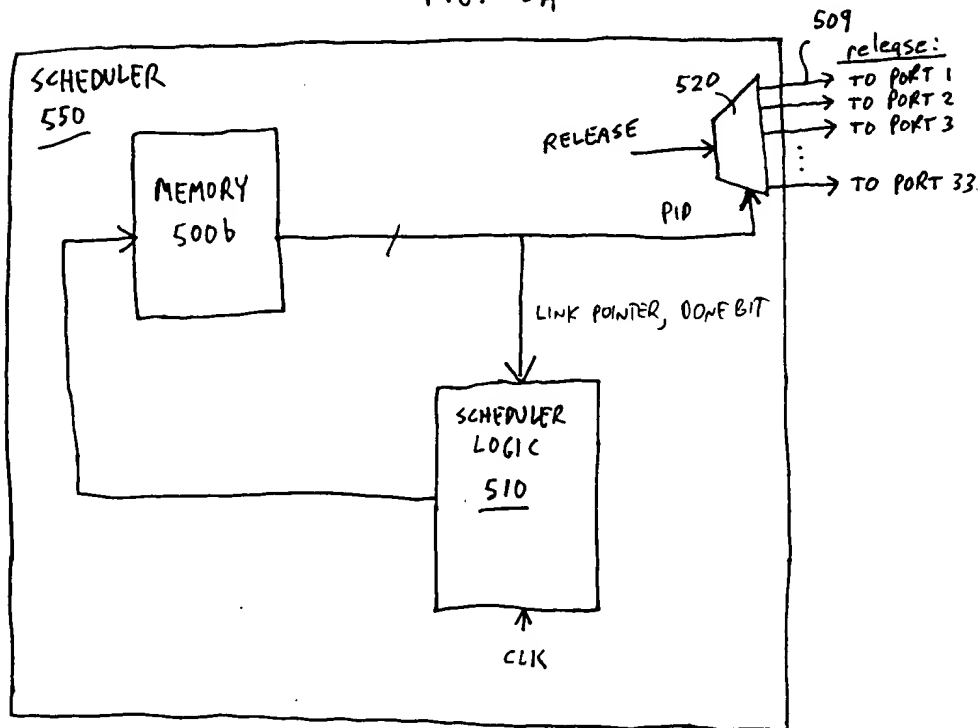


FIG. 5B

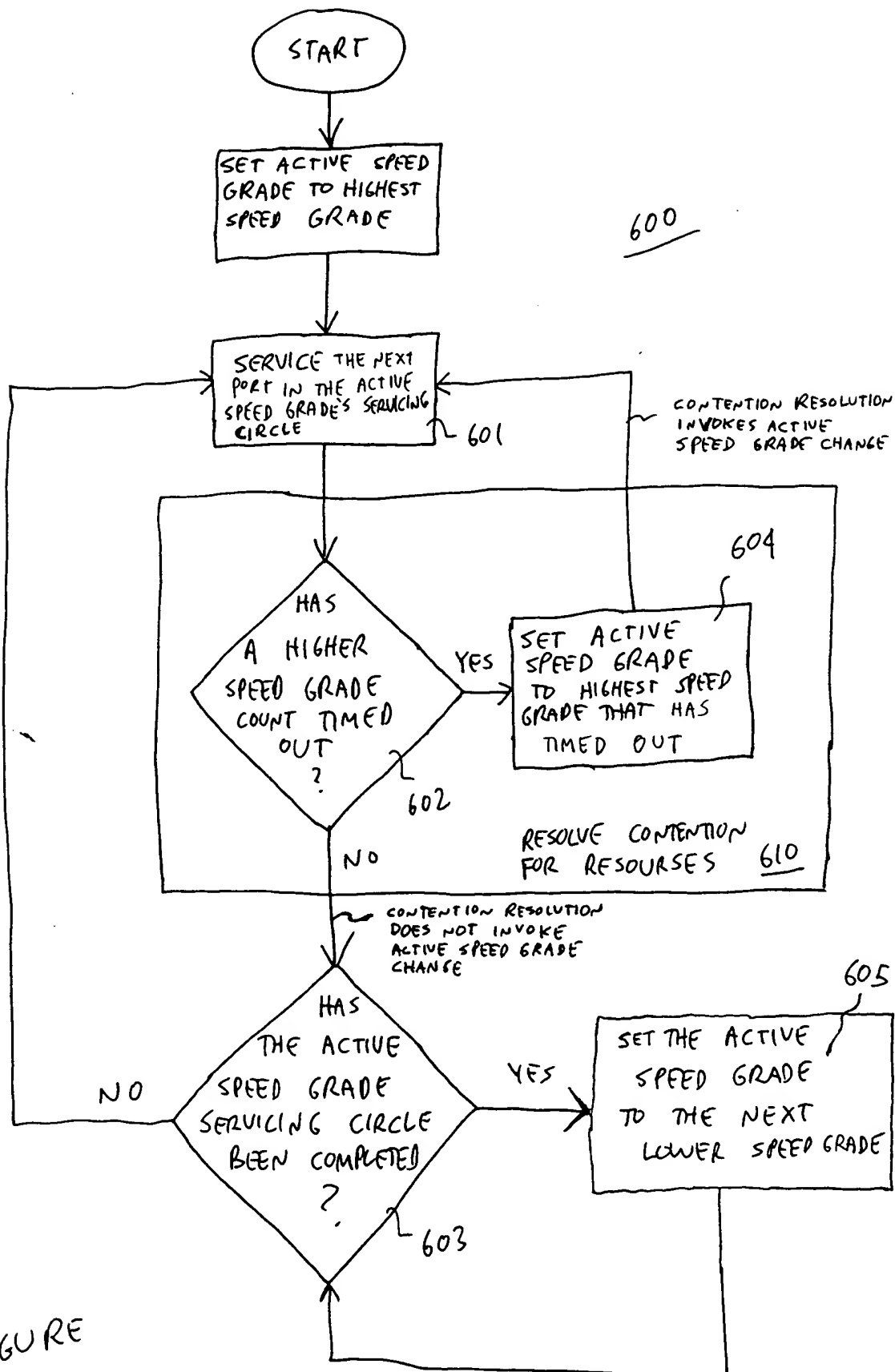


FIGURE
6

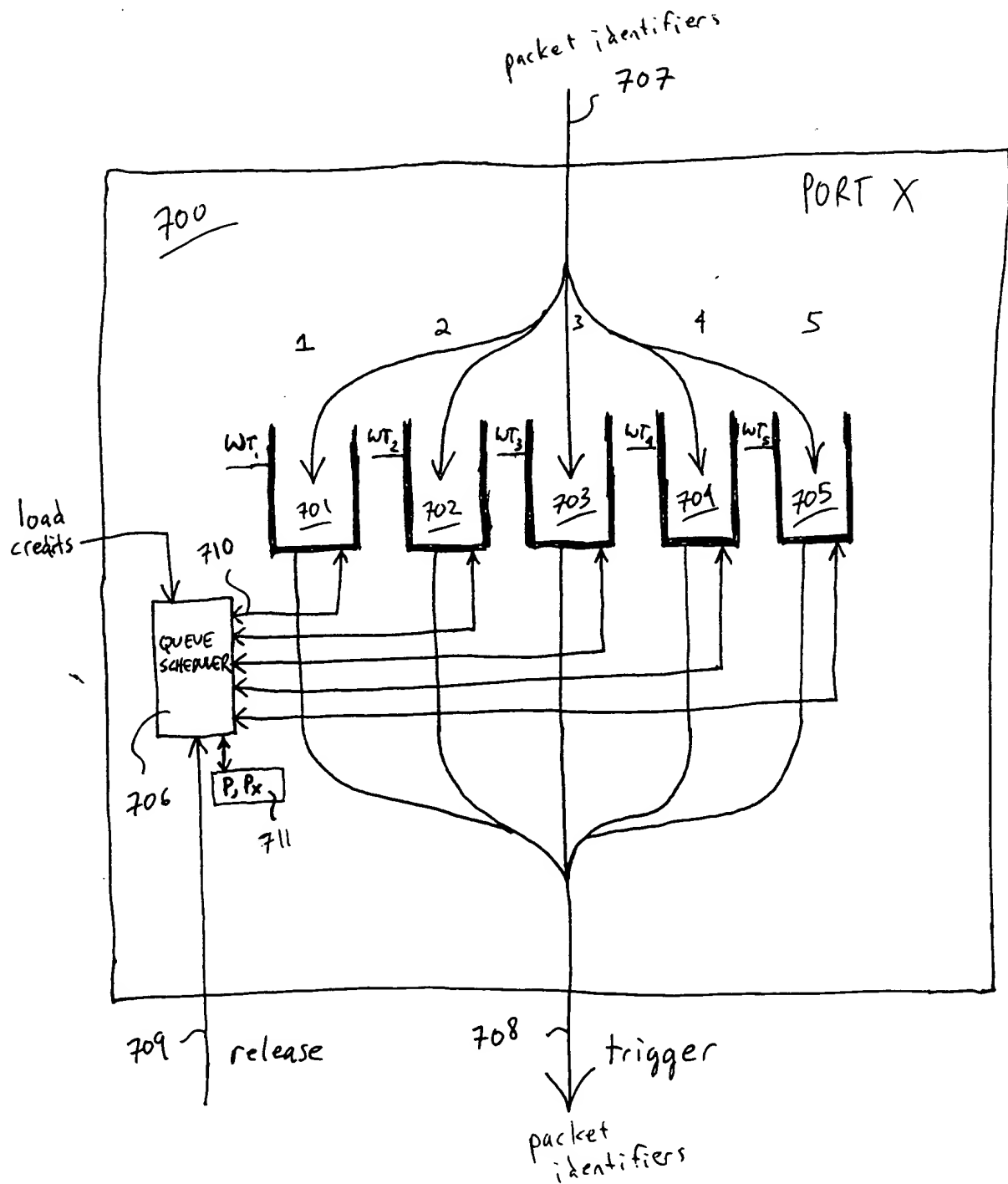
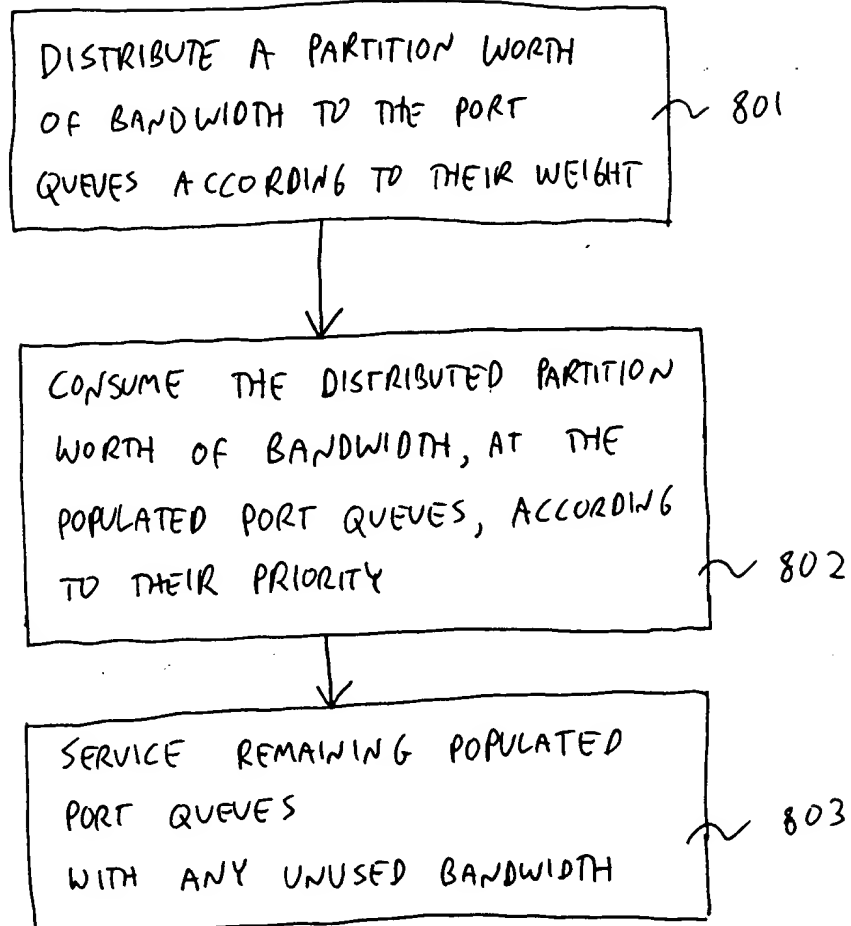


FIGURE 7



800

FIGURE 8

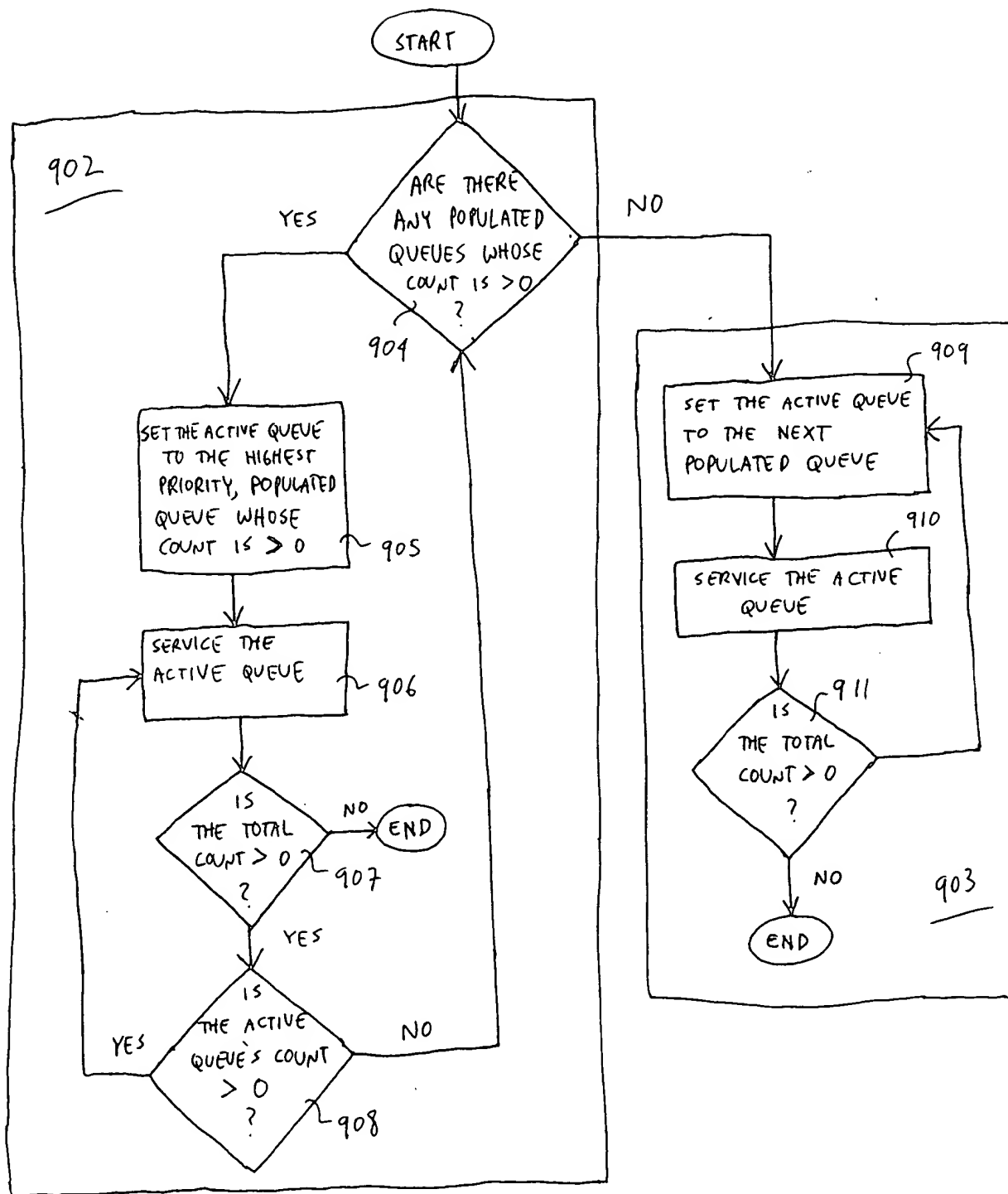


FIGURE 9